Sl No	Particulars		
1	Name of the Candidate	Dr. H.V Ravish Aradhya	
2	Address of the parent institution	R V College of Engineering, 8th Main, Mysore Road, Bangalore 560 059	
3	PhD Thesis Title	Design optimization and Synthesis of low power reversible logic alu components	
4	Research guide Name	Dr K N Muralidhara	
	Department and Designation	Prof and Head, ECE Department	
5	Date of Registration for PhD	Dec- 2006	
	University /Branch	Visvesvaraya Technological University, Belagavi Electrical Engineering Science	
6	Date of Award of PhD degree	20th May 2014	
7	Brief synopsis Power dissipation is a crucial issue today's VLSI system design. Different design abstraction levels in system design offer various power optimization methods. One such methods. One such method at circuit/logic level is reversible logic which is based on energy recovery method. Reversible logic is an emerging research area and provides the advantage of theoretically zero power dissipation. Reversible logic computer is needed to increase the system's rate of computation per unit power consumed. The reversible logic has application is several leading technologies such as quantum computing, quantum dot cellular automata computing, spintronics, conventional CMOS design, adiabatic CMOS design, optical computing, nanotechnology etc. Conventional circuits are irreversible which usually dissipate power. Reversible circuits which are based on reversible logic dissipate nearly zero power. Reversible circuits are built from reversible gates. Reversible gates follow bi-jection function functionality, with one-to-one mapping between the input and output. This means that the number of input is equal to the number of outputs. Unlike conventional logic circuits, reversible logic circuits do not lose information during the entire computation. Reversible gates achieve reversibility through constant 'ancilla inputs' and unused 'garbage output'. The research attempts are made to construct logic circuits which may be implemented in emerging nanotechnology areas.		